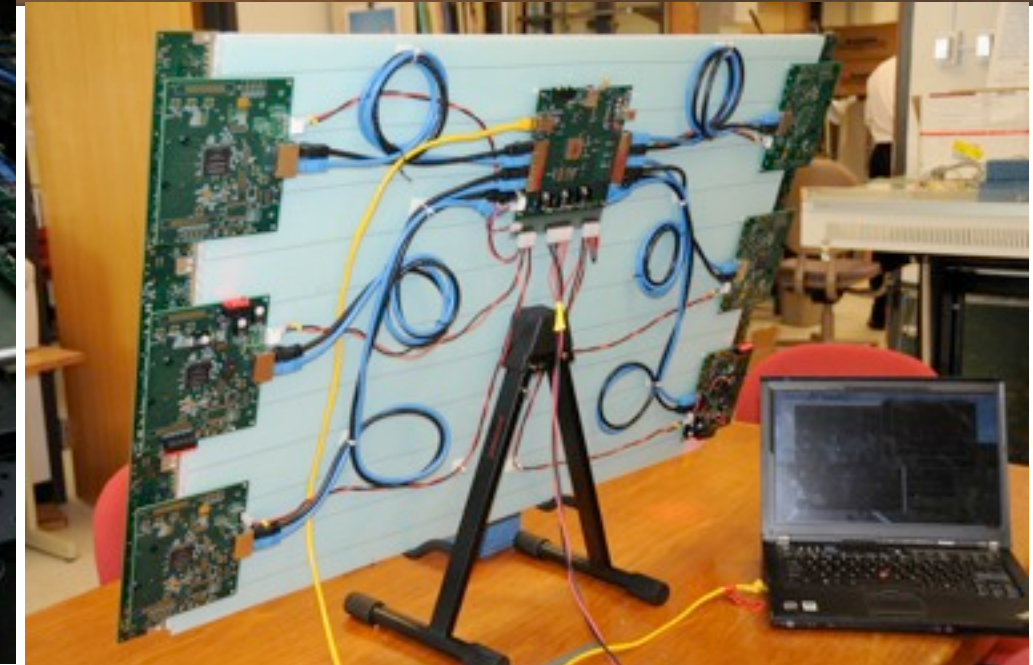
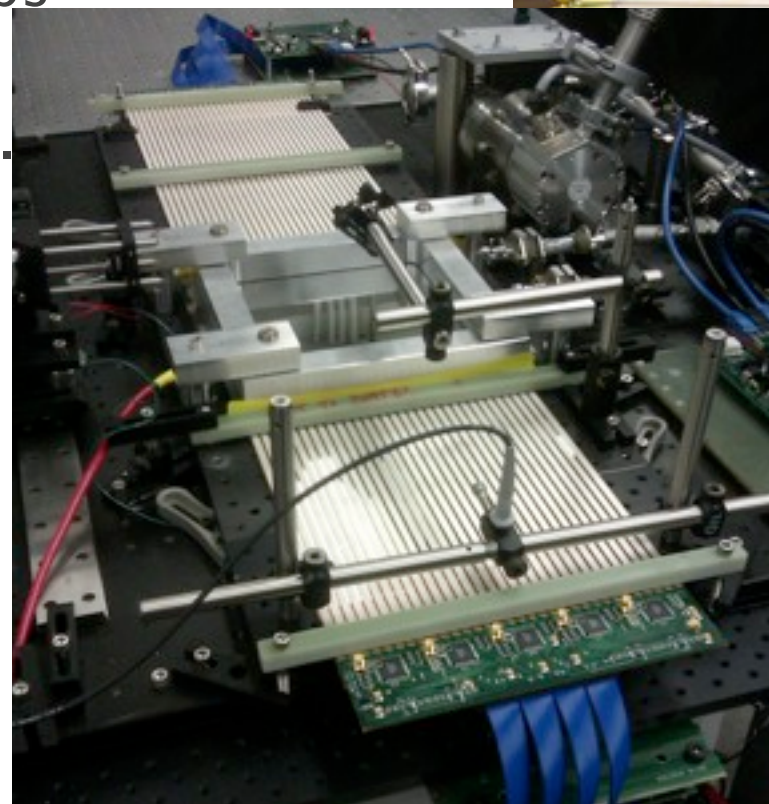
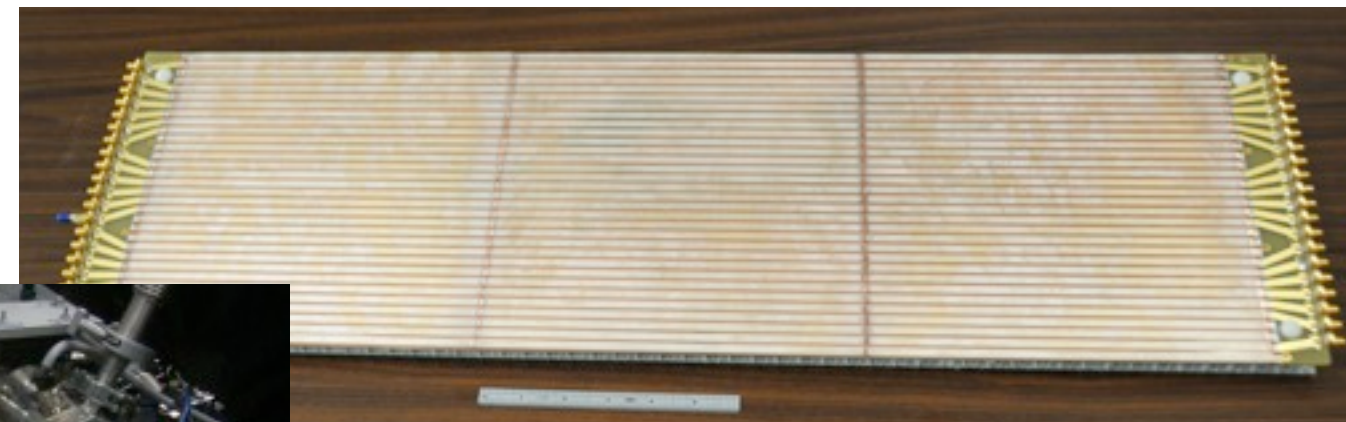
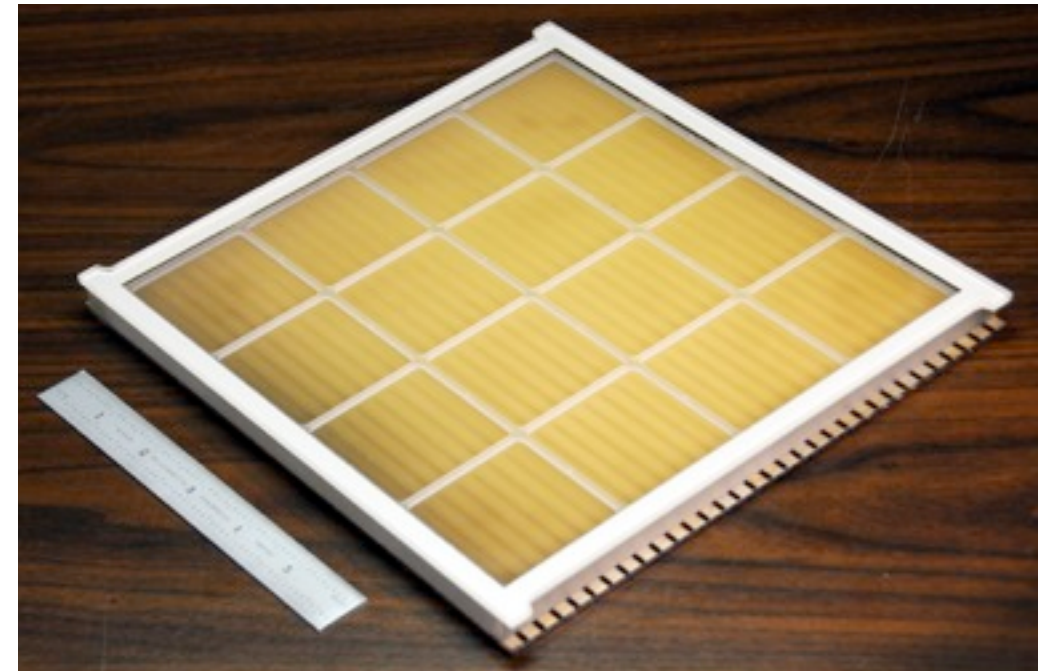


# Integration, Optimization & Support for the Community

Bob Wagner  
LAPPD Collaboration  
Wednesday 19 Dec 2012

# Integration

- ▶ Turning tubes into systems
  - Tube – sealed detector with HV and anode strip, no connectors
  - Instrumentation with ground plane, analog card, digital card, central control
- ▶ Turning systems into useful field systems
  - software/firmware for custom readout electronics
  - calibration of ASIC, tile system
- ▶ on-site support for first adopters
  - rôle to be filled by labs
  - physicist & electronics eng./tech.



Bob Wagner, Argonne, LAPPD2 DOE Review, 19 Dec 2012



# Optimization/Improvement – Performance

- ▶ Photocathode
  - Incremental improvement of existing “recipes”
  - Quantum efficiency of >40%? Via understanding of photocathode material science
- ▶ Microchannel plates see Michael Minot presentation
  - Smaller pore size – increased time & spatial resolution
  - Increased Open Area Ratio (OAR) – p.e. multiplication efficiency, 1<sup>st</sup> strike localization
  - Funneled pore opening – increased OAR, photocathode deposited on funnel?
- ▶ Atomic Layer Deposition (ALD)
  - Determination of optimized ALD physical/chemical parameters for baseline materials
  - Higher Secondary Electron Emission materials
  - Positive thermal coefficient for resistivity – thermal run-away prevention, higher rate capability

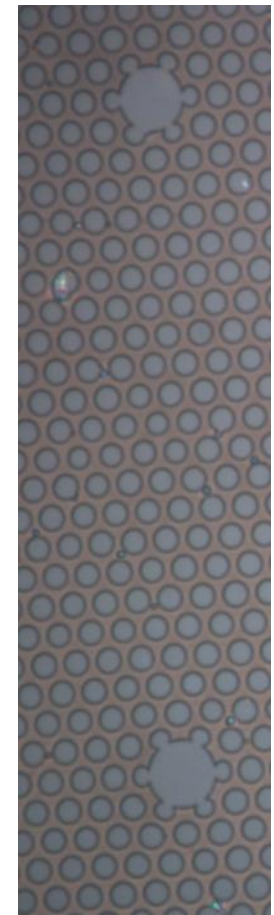


# Optimization/Improvement – Performance (cont.)

- ▶ Anode Strip Line
  - Determine optimum pitch
  - Strip geometry optimization, i.e. width, material, thickness
  - # strips per tile
  - strip line analog band width
- ▶ Readout Improvements
  - Firstly --- Existing readout acceptable for many applications
  - deeper buffered ASIC – 256 sample buffer @ 10 GSa/s  $\Rightarrow$  25 ns coverage
  - Increased analog bandwidth on chip      see Gary Varner's presentation
  - Deadtimeless operation
  - Custom ASICs or FPGA for different applications
  - Increased # channels per control board? (reduce cost per chan.)

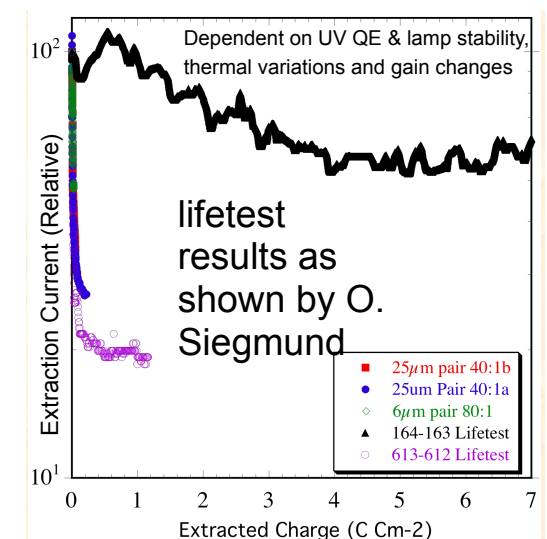
# Optimization/Improvement – Cost

- ▶ Micro-capillary arrays (glass substrates) **ibid** → **Michael Minot**
  - Finishing improvements (yield & performance)
  - Cleaning improvements (yield & performance)
  - larger pores, application dependent
- ▶ Atomic layer deposition process parameters, coating thickness, materials
  - Determine optimum thickness of SEE layers
  - Cheaper (and possibly better) ALD materials
    - $\text{MoF}_6$  (\$26k/kg) vs.  $\text{WF}_6$  (\$800) **better uniformity for lesser price**
    - $\text{Al}_2\text{O}_3$  (TMA @ \$200/100g) vs  $\text{MgO}$  (\$6k/100g) **better performance, higher cost**
- ▶ Glass & ceramic body components
  - Optimize ceramic package fabrication
    - batch processing **see Jason McPhate presentation**
  - Glass
- ▶ Readout
  - FPGA for low rate applications
- ▶ Fabrication methods – tiles
  - tubulation
  - Yield – learn by doing



Ultrasonic  
cleaning  
of MCA

+ 140 kHz



# Community Support

- ▶ Program Goal — Several systems in hands of HEP community during Year 3
- ▶ Year 1 Devices
  - 8” tiles (ceramic and glass) from SSL during Year 1
    - First tiles will stay within Collaboration for evaluation and long term testing
- ▶ Year 2 Devices
  - Provide SSL Fabricated 8” Tiles & Systems to Very Early Adopters
    - Make available tiles/systems with integrated readout and existing analysis software
- ▶ Year 3 Devices – Systems to first adopters by end year 3

Community support from labs will be required for this aspect of the program

